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McDERMONTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
COLEMAN, ERIC	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,866	HANSEN ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 28-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 28-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/27/08, 4/18/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The claims 1-18 and 28-41 are rejected under 35 U.S.C. 112, first paragraph as failing to comply with the description requirement thereof since the claims introduce new matter not supported by the original disclosure. The original disclosure does not reasonably convey to a designer of ordinary skill in the art that applicant was in possession of the design now claimed at the time the application was filed. See *In re Daniels*, 144 F.3d 1452, 46 USPQ2d 1788 (Fed. Cir. 1998); *In re Rasmussen*, 650 F.2d 1212, 211 USPQ 323 (CCPA 1981).

Specifically, there is no support in the original disclosure for the following:

Independent claims 1 now includes the limitation "each of the plurality of mask fields being independently selectable as either write enabled mask field or write-disabled mask field". Claim 28 now includes the limitation " each bit of a second operand is individually selectable as either having a first predetermined value or a second predetermined value. Claim 35 now includes the limitation " wherein each bit in the second operand is individually selectable as either having a first predetermined value or a second predetermined value". This rejection assumes the scope of the claims provides for after the instruction is programmed the individually selecting each of the plural of fields or bits as write enabled or disabled.

These limitations are not described in the application as originally filed. The instructions of the application as originally filed do not provide for mask fields being individually selectable . Note, although claims 28 and 35 provide for operands fields the claims taken as a whole provide for these operands as mask fields. The instructions disclosed in the instant application as originally filed provide for some mask fields or bits which provided as either write enabled and others write disabled but the particular mask bits that are enabled or disabled are not selectable. For a particular instruction the same mask bits are always selected as respectively enabled or disabled the way the instruction was originally programmed. In the instant application as originally filed , there are no disclosed steps for, or mechanism for individually selecting the mask bits for a particular instruction. Therefore Claims 1, 28, 35 (and dependent claims 2-18,29-34 and 36-41) do not meet the description requirement of 112 first paragraph.

To overcome this rejection, applicant may attempt to demonstrate that the original disclosure establishes that he or she was in possession of the amended claims.

Claims 1-18 and 28-41 rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for instructions that have mask bits , does not reasonably provide enablement for provide for mask fields of an instruction being individually selectable. Note that although the wording of claims 28 and 35 provide for operand fields the claims as a whole provide for these operands as mask fields. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to provide and use instructions that include mask bits that are individually selectable the invention commensurate in scope with these claims.

As disclosed the mask for each individual instruction cannot change. So the individual bits that are enable or disabled do not change for an individual instruction. in order to make an use an instruction that additionally provides for individually selectable mask bits would have required alteration of the instructions as disclosed and a mechanism to alter the instruction and provide proper timing for altering and executing the instruction. This would have required undue experimentation to perform and therefore claims 1-18 and 28-41 do not meet the enablement requirement of 35 U.S.C. 112.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1- 8, and 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao (patent No. 4,569,016).

3. Hao taught the invention substantially as claimed including a data processing ("DP") system comprising (as to claim 1): A method for processing data using a programmable processor comprising: Decoding a single processor instruction for writing data to memory based on a mask and data contained in at least one register (e.g. see figs. 2a,2b and col. 25,lines 23-66 and col. 26, lines 3-46), the mask comprising fields that each correspond to a field of the data contained in the at least one register(e.g., see col. 26,lines 36-46); detecting some of the fields of the mask as having a

predetermined value to identify corresponding fields contained in the at least one register as write-enabled data fields(e.g., see col. 26, lines 26-46).

4. Hao did not expressly detail storing the result of a mask in memory. Hao taught storing the write enabled data fields to a specified register (e.g., see col. 13, lines 7-12) and taught the processor performs rotate operations on data from a general purpose register and returns the result, or portion of the result to a general purpose register or to main storage (e.g., see col. 12, lines 42-60). Therefore one of ordinary skill would have been motivated to store the result of the mask and rotate to main storage. The Hao system stores results in main storage and this would have reduced the number of registers needed to perform further processing.

5. Claims 1 includes the limitation: "each of the plurality of mask fields being independently selectable as either write enabled mask field or write-disabled mask field". The fields in the Hao teaching provide individual bits that individually provide for the enabling or disabling of bits of data for write in respective enable or disable status (e.g., see col. 13, lines 5-13). Hao taught a system where a substring within a string is selected using a leftmost index and rightmost index (e.g,. see col. 12, lines 8-29). The indexes comprise a series of bits that indicate the location and boundary within the string of the substring to be masked. The only limitation on the numbers within the indexes are that the rightmost does not exceed the leftmost in value which is an invalid situation. Therefore the situation where the leftmost and rightmost indexes are the same is within the teachings of Hao. This situation would provide a selection of any single bit with the mask string individually depending on what same number the

leftmost and rightmost indexes comprised. Additionally Hao taught a field Bit 21 that indicated whether the selected subfield of the mask comprised a zero or one or correspondingly enabling or disabling write of the bit of the operand (e.g., see col. 12, lines 8-19). Therefore The situation where the leftmost and rightmost indexes have the same value provide for a mask where Bit 21 indicates the value of an individually selected bit of the mask for selecting whether to enable or disable writing the corresponding single bit of the operand.

6. As per claim 2, Hao taught each of the fields of the mask has a width of one bit (e.g., see col. 15, lines 39-44).

7. As per claim 3, Hao taught each of the fields of data contained in the at least one register has a width of one bit (e.g., see col. 15, lines 39-44).

8. As per claim 4, Hao taught the writing step further comprises reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields of the specified memory location (e.g., see col. 15, lines 39-44).

9. As per claim 5, Hao taught the mask is contained in a specified register (e.g., see col. 28, lines 21-54).

10. As per claim 6, Hao taught storing the result a memory location (e.g., see col. 12, lines 42-60). Therefore one of ordinary skill would have been motivated to provide the destination memory location in a register such as the instruction register when the destination address an immediate field or another register when the destination was specified using direct or indirect addressing.

11. As per claim 7, Hao taught the architecture comprising a 32-bit architecture (e.g,. see col. 8, lines 64-68). Therefore one of ordinary skill would have been motivated to store the data or instructions to memory in specified memory locations comprises a section of memory having a specific width (e.g., 32-bits) and beginning at a specific memory address at least to allow later retrieval of stored data.

12. As per claim 8, Hao taught the predetermined logic value is 1(e.g. see col. 13, lines 6-15).

13. As per claim 10, Hao taught computer readable storage medium (main storage, and I-cache (e.g., see fig.1) stored therein a plurality of instructions that cause programmable processor to perform data operations: at least some of the instructions including a single instruction for selectively storing the single instruction capable of instructing the programmable processor to perform operations (e.g., see col. 12, line 56-col. 22, line 64) comprising: decoding the single instruction to obtain a mask and data contained in at least one register (e.g. see figs. 2a, 2b and col. 25,lines 23-66 and col. 26, lines 3-46), the mask comprising fields that each correspond to a field of the data contained in the at least one register e.g., see col. 26,lines 36-46); detecting some of the fields of the mask as having a predetermined value to identify corresponding fields of the data contained in the at least one register as write-enabled data fields (e.g., see col. 26, lines 26-46). Hao did not expressly detail storing the result of a mask in memory. Hao taught storing the write enabled data fields to a specified register (e.g., see col. 13, lines 7-12) and taught the processor performs rotate operations on data from a general purpose register and returns the result, or portion of the result to a

general purpose register or to main storage (e.g., see col. 12, lines 56-60). Therefore one of ordinary skill would have been motivated to store the result of the mask and rotate to main storage. The Hao system stores results in main storage and this would have reduced the number of registers needed to perform further processing.

14. As per claim 11, Hao taught each of the fields of the mask has a width of one bit(e.g., see col. 15, lines 39-44)..

15. As per claim 12, Hao taught each of the fields of the data contained in the at least one register has a width of one bit (e.g., see col. 15, lines 39-44).

16. As per claim 13, Hao taught the writing step comprises reading a unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location (e.g., see col. 15, lines 39-44).

17. As per claim 14, Hao taught the mask is contained in a specified register (e.g., see col. 28, lines 21-54).

18. As per claim 15, Hao taught storing the result a memory location (e.g., see col. 12, lines 42-60). Therefore one of ordinary skill would have been motivated to provide the destination memory location in a register such as the instruction register when the destination address an immediate field or another register when the destination was specified using direct or indirect addressing.

19. As per claim 16, Hao taught the architecture comprising a 32-bit architecture (e.g., see col. 8, lines 64-68). Therefore one of ordinary skill would have been motivated to store the data or instructions to memory in specified memory locations

comprises a section of memory having a specific width (e.g., 32-bits) and beginning at a specific memory address at least to allow later retrieval of stored data.

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20. As per claim 17, Hao taught the predetermined value is 1(e.g. see col. 13, lines 6-15).

21. Claims 9,18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao applied to claims 1-8,10 above, and further in view of Kabir (patent No. 5,933,160).

22. As per claim 9, 18 Kabir taught decoding a second single instruction specifying a fourth register containing a plurality of floating point operands; multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality of products; and providing the partitioned field of a result as a concatenated result (e.g., see fig. 4, 5a, 5b and col. 8,lines 21-45).

23. It would have been obvious to one of ordinary skill to combine the teachings of Hao and Kabir. Both references were directed toward performing operations of partial widths of data stored in registers. Kabir taught further operations to be performed on the partial width data such as multiplication on floating point data (e.g., see fig. 4) for performing image processing in a digital system (e.g., see col. 1, lines 6-11) consequently one of ordinary skill would have been motivated to incorporate the floating point operations to the Hao system at least to provide the capability use in addition applications such as graphics applications.

24. Claims 28-32 and 35-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Hao et al. (patent No. 4,569,016).

25. As per claims 28, Hao taught a method for processing in a programmable processor the method comprising: Decoding a single instruction for performing a bitwise insert operation on data in at least one register in a register file within the programmable processor (e.g. see figs. 2a,2b and col. 25,lines 23-66 and col. 26, lines 3-46), the bitwise insert operation operating on a first operand and a second operand stored in the at least one register (e.g., see col. 26, lines 36-46); and for each bit in the first operand, the bitwise insert operation inserting the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has a first predetermined value (e.g., see col. 15, lines 39-44).

26. Claims 28 includes the limitation: "each bit in the second operand is individually selectable as either having a first predetermined value or a second predetermined value and for each bit in the first operand, the bitwise insert operation inserting the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has the first predetermined value" The fields in the Hao teaching provide individual bits that individually provide for the enabling or disabling of bits of data for write in respective enable or disable status (e.g., see col. 13, lines 5-13). Hao taught a system where a substring within a string is selected using a leftmost index and rightmost index (e.g,. see col. 12, lines 8-29). The indexes comprise a series of bits that indicate the location and boundary within the string of the substring to be masked. The only limitation on the numbers within the indexes are that the rightmost does not exceed the leftmost in value which is an invalid situation. Therefore the situation where the leftmost and rightmost indexes are the same is within the teachings of Hao. This

situation would provide a selection of any single bit with the mask string individually depending on what same number the leftmost and rightmost indexes comprised. Additionally Hao taught a field Bit 21 that indicated whether the selected subfield of the mask comprised a zero or one for correspondingly enabling or disabling write of the bit of the operand (e.g., see col. 12, lines 8-19). Therefore The situation where the leftmost and rightmost indexes have the same value provide for a mask where Bit 21 indicates the value of an individually selected bit of the mask for selecting whether to enable or disable writing the corresponding single bit of the operand.

27. As per claim 29, Hao taught the first predetermined value is a logic 1 (e.g. see col. 13, lines 6-15).

28. As per claim 30, Hao taught for each bit in the first operand, a corresponding bit position in the destination value is maintained as unchanged if a corresponding bit in the second operand has a second predetermined value (e.g., see col. 15, lines 39-44).

29. As per claim 31, Hao taught the second predetermined value is 0 (e.g. see col. 13, lines 6-15).

30. As per claim 32, Hao taught storing the destination value result a memory location (e.g., see col. 12, lines 42-60).

31. As per claim 35, Hao taught A computer readable medium having stored therein a plurality of instructions that cause a programmable processor to perform operations on data stored in the programmable processor(e.g. see figs. 2a,2b and col. 25,lines 23-66 and col. 26, lines 3-46), the plurality of instructions comprising: an instruction that causes the processor to perform a bitwise insert operation on data in at least one

register (e.g., see col. 26, lines 36-46) within the programmable processor, the bitwise insert operation operating on a first operand and a second operand stored in the at least one register in the register file; and wherein for each bit in the first operand, the bitwise insert operation inserts the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has a first predetermined value(e.g., see col. 15, lines 39-44).

32. Claims 35 includes the limitation: "each bit in the second operand is individually selectable as either having a first predetermined value or a second predetermined value and wherein for each bit in the first operand, the bitwise insert operation inserts the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has the first predetermined value". The fields in the Hao teaching provide individual bits that individually provide for the enabling or disabling of bits of data for write in respective enable or disable status (e.g., see col. 13, lines 5-13). Hao taught a system where a substring within a string is selected using a leftmost index and rightmost index (e.g,. see col. 12, lines 8-29). The indexes comprise a series of bits that indicate the location and boundary within the string of the substring to be masked. The only limitation on the numbers within the indexes are that the rightmost does not exceed the leftmost in value which is an invalid situation. Therefore the situation where the leftmost and rightmost indexes are the same is within the teachings of Hao. This situation would provide a selection of any single bit with the mask string individually depending on what same number the leftmost and rightmost indexes comprised. Additionally Hao taught a field Bit 21 that indicated whether the selected subfield of the

mask comprised a zero or one for correspondingly enabling or disabling write of the bit of the operand (e.g., see col. 12, lines 8-19). Therefore The situation where the leftmost and rightmost indexes have the same value provide for a mask where Bit 21 indicates the value of an individually selected bit of the mask for selecting whether to enable or disable writing the corresponding single bit of the operand.

33. As per claim 36, Hao taught the first predetermined value is 1(e.g. see col. 13, lines 6-15).

34. As per claim 37, Hao taught for each bit in the first operand, a corresponding bit position in the destination value is maintained as unchanged if a corresponding bit in the second operand has a second predetermined value (e.g., see col. 15, lines 39-44).

35. As per claim 38, Hao taught the predetermined logic value is 0(e.g. see col. 13, lines 6-15).

36. As per claim 39, Hao taught the destination value is stored into memory (e.g., see col. 12, lines 42-60).

37. Claims 33,34,40,41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao as applied to claims 28,35 above, and further in view of Kabir.

38. As per claims 33,40 Kabir taught arithmetic operation where operands were stored in registers of 64-bit width (e.g., see col. 8, lines 5-37 and col. 9, line 27-col. 10, line 28 and fig.5A,5B). As to the operand being 64 bit width one of ordinary skill would have been motivated to use data with more bits such as 64, 128 etc to take advantage of the increasing capacity of industry standard memories, data paths and processors at the time of the claimed invention.

39. It would have been obvious to one of ordinary skill to combine the teachings of Hao and Kabir. Both references were directed toward performing operations of partial widths of data stored in registers. Kabir taught further operations to be performed on the partial width data such as multiplication on floating point data (e.g., see fig. 4) for performing image processing in a digital system (e.g., see col. 1, lines 6-11) consequently one of ordinary skill would have been motivated to incorporate the floating point operations to the Hao system at least to provide the capability use in addition applications such as graphics applications.

40. As per claim 34, Kabir taught executing a plurality of different group floating point operation that arithmetically operate on multiple floating point operands partitioned in fields of an operand register in the plurality of registers to produce a concatenated result that is returned to a register in the plurality of registers, wherein the concatenated result comprises a plurality of individual floating point results (e.g., see fig. 4, 5a, 5b and col. 8,lines 21-45 and col. 5, lines 6-47 and col. 4, lines 23-64).

41. As per claim 41, Kabir taught instructions further comprises a plurality of different group floating-point arithmetic operations that arithmetically operate one multiple floating-point operands stored in partitioned fields of an operand register in the plurality of registers to produce a concatenated result that is returned to a register in the plurality of registers, wherein the concatenated result comprises a plurality of individual floating-point results (e.g., see col. 4, lines 23-61 and col. 7, line 7-col. 8, line 41).

Response to Arguments

Applicant's arguments with respect to claims 1-18, 28-41 have been considered but are moot in view of the new ground(s) of rejection.

Note the 6,295,599 and 5,742,840 patents argued by the Applicant are not deemed to provide support for the claims in the instant application as described in the 112 first paragraph rejection above. The instructions cited in the remarks, are deemed as performing an operation that is set and the bits that are masked are predetermined and which bits are to be enabled or disabled for write are predetermined and set. The Applicant cited instructions in '599 and '840 patents do not provide for individually selecting a bit of an operand of an operand for enabling or disabling write of the bits during processing of the instruction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC
/Eric Coleman/
Primary Examiner, Art Unit 2183